

Abstract

Quasi-one dimensional nanostructures such as semiconductor nanowires and carbon nanotubes (CNT) have unique mechanical and electronic properties are currently under investigation for nanoelectronic technology generations beyond the 14 nm node. Semiconductor nanowires are readily integrated into electronic systems using top down lithography. Recently, Intel has announced the “tri-gate” field effect transistor, a silicon nanowire structure, in their recently released Ivy Bridge processors. Field effect transistors (FETs) are the building block used as the basis for random-access memory, flash memory, processors, and application-specific integrated circuits (ASICs), in short they are the building blocks for most modern integrated circuits. Nanoscale FETs enable the continuation of the Moore’s law for future technology generations, permit higher device density and consequently high function per integrated circuit at lower unit cost. Critically, use of nanowire transistors permit efficient electrostatic control over charges in the nanowires to allow for low power nanoelectronics, that are now required at the heart of all mobile applications such as smart phones and tablets.

The aim of this study is to build on previous simulations based on a fully atomistic and quantum mechanical description of charges in nanowires by extending the study to include three new materials: germanium, tin, bismuth as potential channel materials in nanoscale FETs. It is not a foregone conclusion that silicon will remain the material of choice below 5 nm technology nodes, and these simulations are designed to explore and compare the relative merits of alternative channel materials. To achieve this aim, atomic models of nanowires will be constructed with diameters up to 6 nanometres and their electronic behaviour described using density functional theory (DFT). The first step in the calculations is to obtain relaxed structures and the band structures for the nanowires. The DFT calculated Hamiltonians for the nanowires are then coupled into a simulation tool that mimics connecting the nanowires to a voltage source (open system boundary conditions) to allow the investigation of current flow in nanowire transistors. For realistic transistor structures on the order of one thousand atoms must be included in the DFT calculations to determine the scattering region (channel) Hamiltonian matrices that are applied in conjunction with electrode self-energies in a Green’s function calculations of electron transport. This large number of atoms treated by DFT electronic structure codes (discussed under Methodology) places a large demand on the memory requirements per core, therefore, Stoney which can provide larger amount of memory (up to 6 GB/core) is required. Our ab-initio calculations performed for SiNWs and CNTs on the Stoney cluster demonstrate that this large memory requirements is needed, motivating our request to use Stoney to extend the material sets (Ge, Sn, Bi) under consideration for FET channel materials for end-of-the-roadmap electronics.